Daala-TX

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What is Daala TX

Replaces the existing AV1 TX with the lifting implementation from Daala.

Type-II 4-point DCT

Type-IV 4-point DST
Daala TX

Daala TX is a better implementation in every way...

- Lower operation count, fewer multiplies
  - complete multiply/downshift/round is a single instruction (VQRDMULH in NEON, PMULHRSW in SSSE3)
  - no halving of the SIMD throughput during the rotations

- Orthonormal scaling
  - No need for different shifts at different transform sizes
  - Use same quantizers for all transform sizes and depths

- Smaller intermediaries
- Daala 'low-bitdepth' transforms wide enough for high-bitdepth

- Deeper noise floor
  - Increase coefficient shift for more gain (.5%-1%)

- Reusable / embedded design (less hardware area)
- Inherently lossless
Arithmetic dependency depth

The One Disadvantage: Multiplies are partly serialized
Arithmetic depth (2)

The solution: Hybrid transforms
Use where hardware latency is critical

Factorization structure for type-VII 4-point DST

Tradeoff: Hybrid TX loses inherent invertibility/losslessness
Daala TX: Current State

Landed or pending review:

- All transforms in place, active in lowbitdepth path (CONFIG_DAALA_TX)
- Optional hybrid 4-point DST-VII (Gerrit 19021)

To do:

- High bit-depth glue code
- Move AV1 to same-quantizer for all TX sizes and depths
- Decisions (use low-latency hybrid or no?)
Questions?